CLAIMS

1. Non volatile memory device architecture, for example of the Flash type, incorporating a memory cell matrix and an input/output interface for receiving memory data and/or addresses from and to the outside of the device, said interface operating according to a serial communication protocol, characterised in that it comprises in said interface a further pseudo-parallel communication portion having a low pin number and incorporating circuit blocks for selecting the one or the other communication mode against an input-received selection signal.

2. Architecture according to claim 1, characterised in that said circuit blocks comprise at least a state machine receiving a clock signal and a selection signal for activating the remaining blocks; an instruction decoder block for decoding in the SPI serial mode the various communication protocol commands and an enabling signal generator block for loading data and address registers.

3. Architecture according to claim 2, characterised in that said interface comprises also a latch register block to store temporarily input and output addresses on address pins.

4. Architecture according to claim 1, characterised in that said interface comprises also a latch register block to store temporarily input and output data on data pins.

5. Architecture according to claim 3, characterised in that said address latch registers are at least twenty-four.

6. Architecture according to claim 4, characterised in that said data latch registers are at least eight.

7. Architecture according to claim 3, characterised in that said address register block is associated to an enabling pulse generator block to generate latching pulses based on the logic value of a signal received by said signal generator block and it selects which one of the two serial or pseudo-parallel interface is to be used.

8. Architecture according to claim 4, characterised in that said data register block is associated to an enabling pulse generator block to generate latching pulses based on the logic value of a signal received by said signal generator block and it selects which one of the two serial or pseudo-parallel interface is to be used.

9. Architecture according to claim 1, characterised in that said signal generator block produces at least the following signals: SPI_EN_ADD<21:0> for enabling an address bit latching in the SPI serial mode; each pulse stores a sole address bit; SPI_EN_DATA<7:0> for enabling the serial generation of the output datum; COL_PULSE to store in the pseudo-parallel mode the content of the addresses in a register block as the less significant part; ROW_PULSE to store the content of the addresses in a register block as the most significant part; DQ_PULSE to generate output data still in the pseudo-parallel mode.

10. Architecture according to claim 1, characterised in that it comprises eleven address pins for the address flow in the pseudo-parallel mode, one of them being used as input pin in the serial mode, as well as eight data pins for the pseudo-parallel mode, one of them being used as the output pin in the SPI serial mode.

11. A method of operating a memory device incuding a matrix of memory cells, comprising:

during a normal mode of operation,

serially receiving address bits on a pin of the memory device;

sequentially latching the address bits;

accessing memory cells in the matrix that correspond to the the latched address bits; and

serially providing bits of data stored in the accessed memory cells onto a pin of the memory device; and

during a test mode of operation,

receiving and storing a plurality of address bits in parallel, the bits being applied on respective pins of the device;

accessing memory cells in the matrix that correspond to the the stored address bits; and

providing in parallel bits of data stored in the accessed memory cells onto pins of the memory device.

12. The method of claim 11 wherein the test mode of operation comprises an electrical wafer sort test mode.

13. The method of claim 11 wherein receiving and storing a plurality of address bits in parallel comprises receiving and storing a column address including a plurality of bits and receiving and storing a row address including a plurality of bits.

14. The method of claim 11 wherein at least some of the respective pins of the memory device on which the plurality of address bits are received in the test mode are not accessible during the normal mode of operation.

15. A memory device, comprising:

a matrix of memory cells; and

an interface coupled to the matrix of memory cells and coupled to pins of the memory device, the interface operable in a serial mode responsive to control signals applied on respective pins to serially receive addresses and data and to provide these addresesses and data in parallel form to the matrix of memory cells, and operable in a parallel mode responsive to the control signals to receive parallel address and data applied on external pins and to apply this data in parallel form tot he matrix of memory cells.

16. The memory device of claim 15 wherein the interface operates in the serial mode during normal operation of the memory device and wherein the interface

operates in the parallel mode during a testing of the memory device.

17. The memory device of claim 15 wherein the matrix of memory cells comprises a matrix of flash memory cells.

18. The memory device of claim 15 wherein the interface comprises:

a plurality of latches operable to serially latch address bits applied on an external pin of the device;

a data output circuit operable to receive a parallel data word from the matrix to serially output bits of this data word during the serial mode and to output the bits in parallel during the parallel mode;

a control circuit operable responsive to control signals applied on external pins to apply control pulses to the latches and data output circuit to control the circuit during the serial and parallel modes;

an instruction decoder operable operable in the serial mode to serially receive address bits applied on a respective pin of the device and to decode the serially received bits to develop a corresponding serial mode command that is utilized in controlling the data output and control circuits; and

a state machine operable to receive the control signals applied to the control circuit to apply enable signals to latches, data output circuit, control circuit, and instruction decoder.

19. The memory device of claim 15 wherein the device further comprises a package that houses the matrix and the interface and that includes a plurality of external pins coupled to the interface, and wherein at least some of the pins utilized by the interface during the parallel mode are not coupled to external pins of the package.

20. A computer system comprising computer circuitry coupled to a memory device, the memory device including,

a matrix of memory cells; and

an interface coupled to the matrix of memory cells and coupled to external pins of the memory device, the interface operable in a serial mode responsive to control signals applied on respective pins to serially receive addresses and data and to provide these addresesses and data in parallel form to the matrix of memory cells, and operable in a parallel mode responsive to the control signals to receive parallel address and data applied on external pins and to apply this data in parallel form tot he matrix of memory cells.

21. The computer system of claim 20 wherein the memory device comprises a flash memory device.

22. The computer system of claim 20 wherein the interface operates in the serial mode during normal operation of the memory device and wherein the interface operates in the parallel mode during a testing of the memory device.

23. The computer system of claim 20 wherein the memory device further comprises a package that houses the matrix and the interface and that includes a plurality of external pins coupled to the interface, and wherein at least some of the pins utilized by the interface during the parallel mode are not coupled to external pins of the package.

24. The computer system of claim 20 wherein the interface comprises:

a plurality of latches operable to serially latch address bits applied on an external pin of the device;

a data output circuit operable to receive a parallel data word from the matrix

to serially output bits of this data word during the serial mode and to output the bits in parallel during the parallel mode;

a control circuit operable responsive to control signals applied on external pins to apply control pulses to the latches and data output circuit to control the circuit during the serial and parallel modes;

an instruction decoder operable operable in the serial mode to serially receive address bits applied on a respective pin of the device and to decode the serially received bits to develop a corresponding serial mode command that is utilized in controlling the data output and control circuits; and

a state machine operable to receive the control signals applied to the control circuit to apply enable signals to latches, data output circuit, control circuit, and instruction decoder.